Appendix B: Formal Drawings

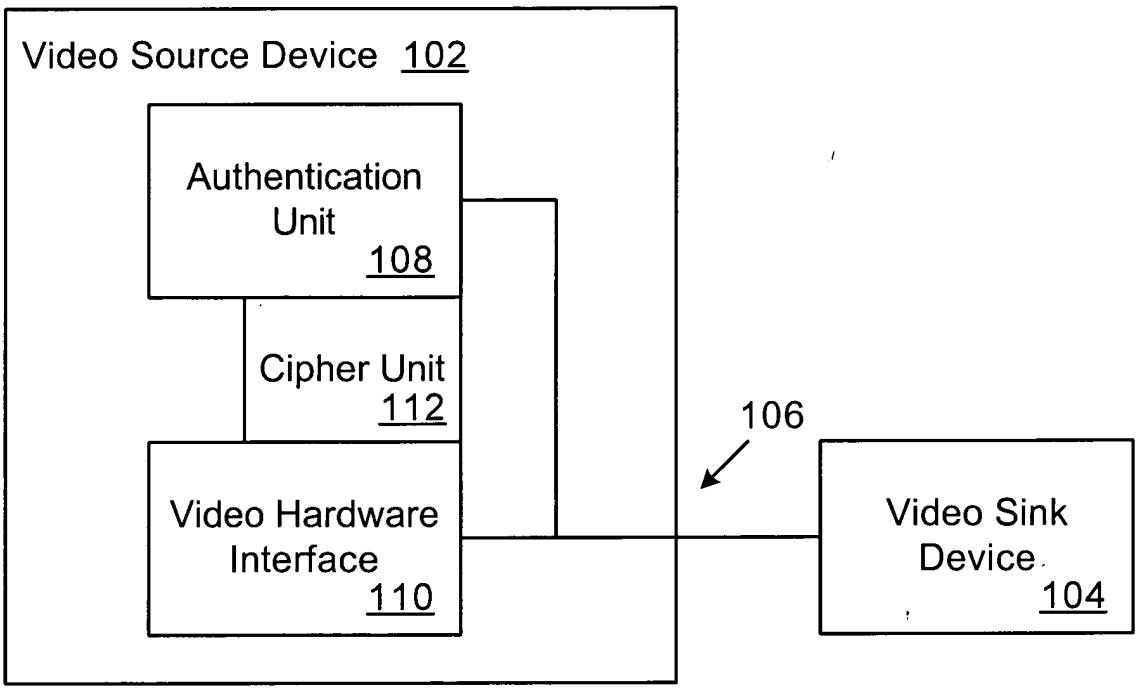

FIG. 1

Video Source Device (Ak_{sv})		Video Receiving Device (Bk_{sv})
Generate A_n	A_n, Ak_{sv} → ; ← Bk_{sv}	
Generate K_m (Ak_{sv}, Bk_{sv}) Generate K_s, M_0, R_0 (K_m, A_n)		Generate K_m (Ak_{sv}, Bk_{sv}) Generate K_s, M_0, R_0 (K_m, A_n)
Determine if $R_0 = R_0$	← R_0	

FIG. 2

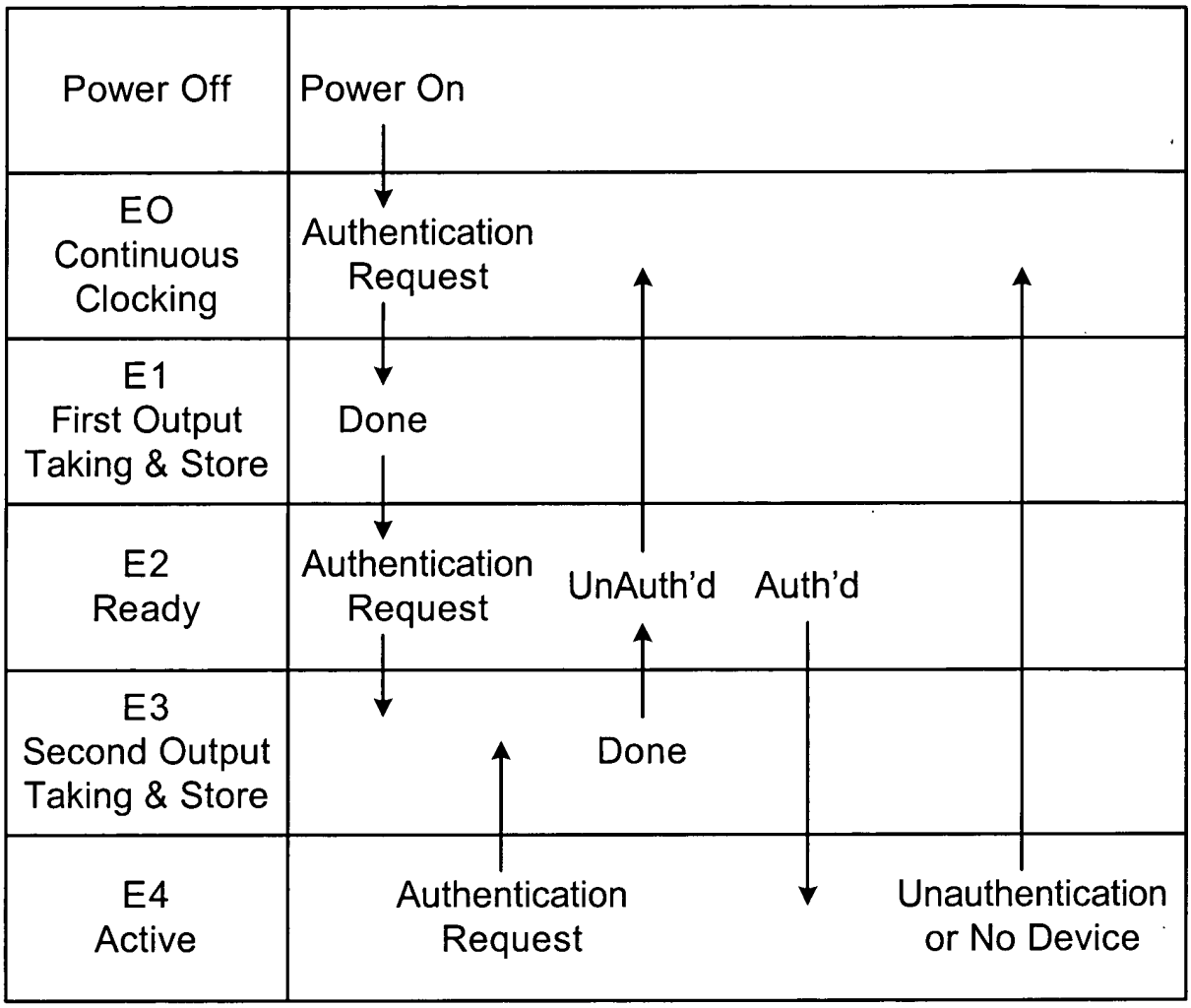

FIG. 3

800

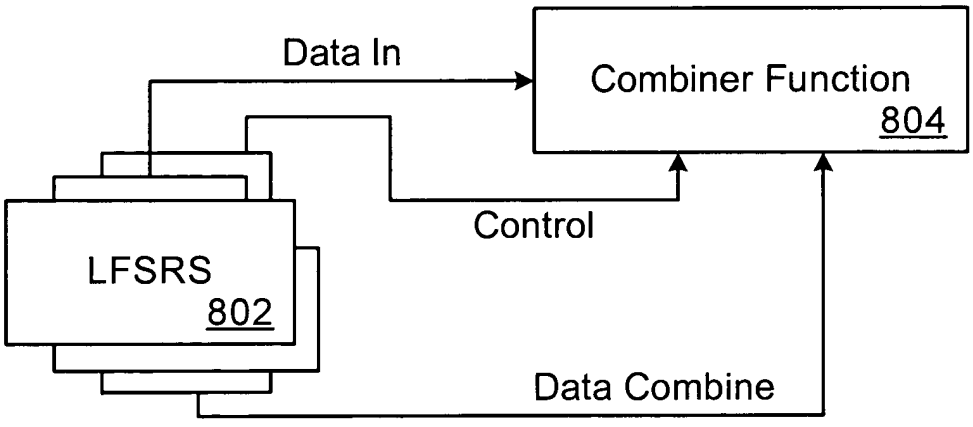

FIG. 4a

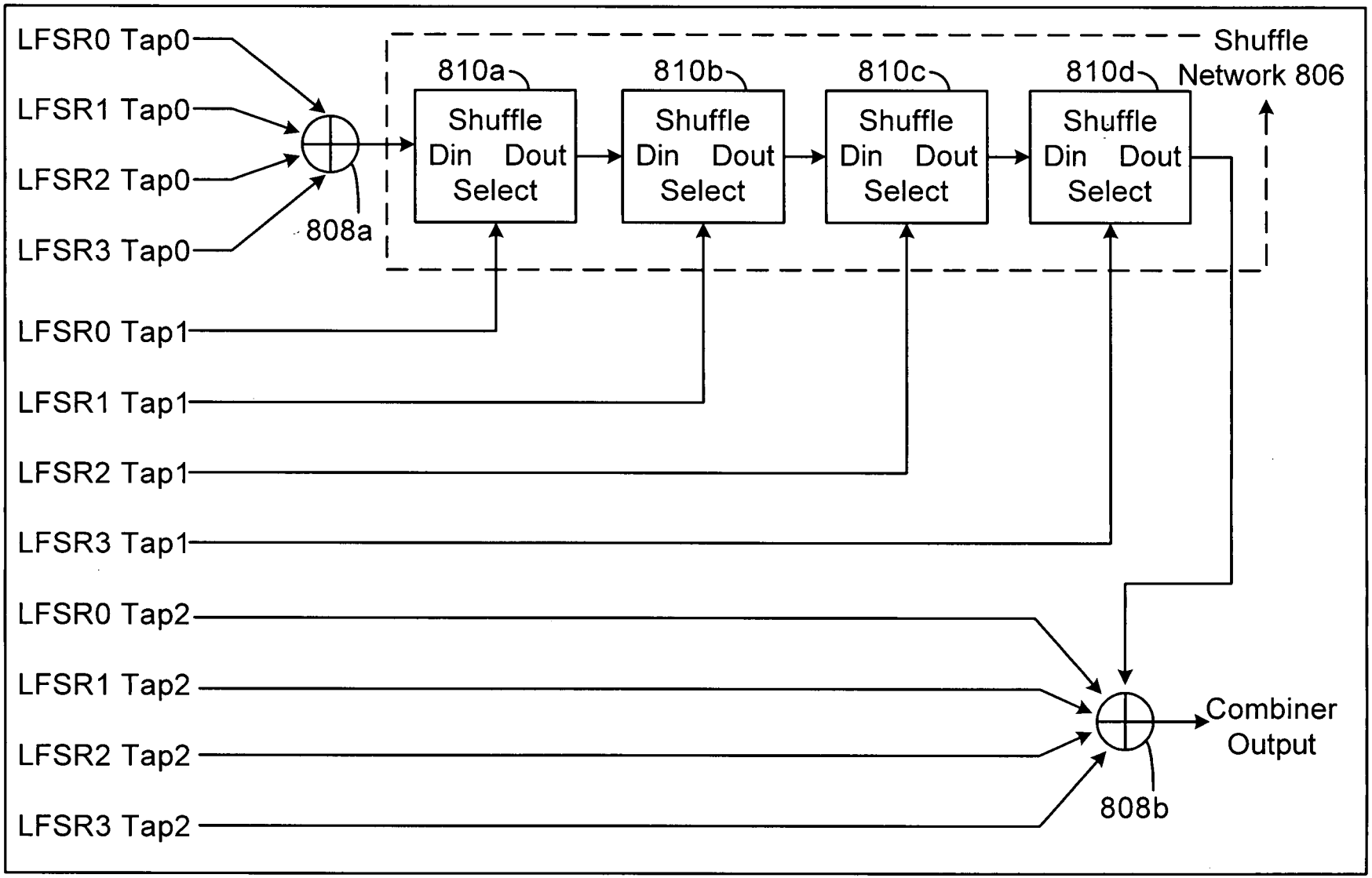
LFSR0 Tap0
LFSR1 Tap0
LFSR2 Tap0
LFSR3 Tap0
808a
810a
Shuffle
Din Dout
Select
810b
Shuffle
Din Dout
Select
810c
Shuffle
Din Dout
Select
810d
Shuffle
Din Dout
Select
Shuffle
Network 806
LFSR0 Tap1
LFSR1 Tap1
LFSR2 Tap1
LFSR3 Tap1
LFSR0 Tap2
LFSR1 Tap2
LFSR2 Tap2
LFSR3 Tap2
Combiner
Output
808b

FIG. 4b

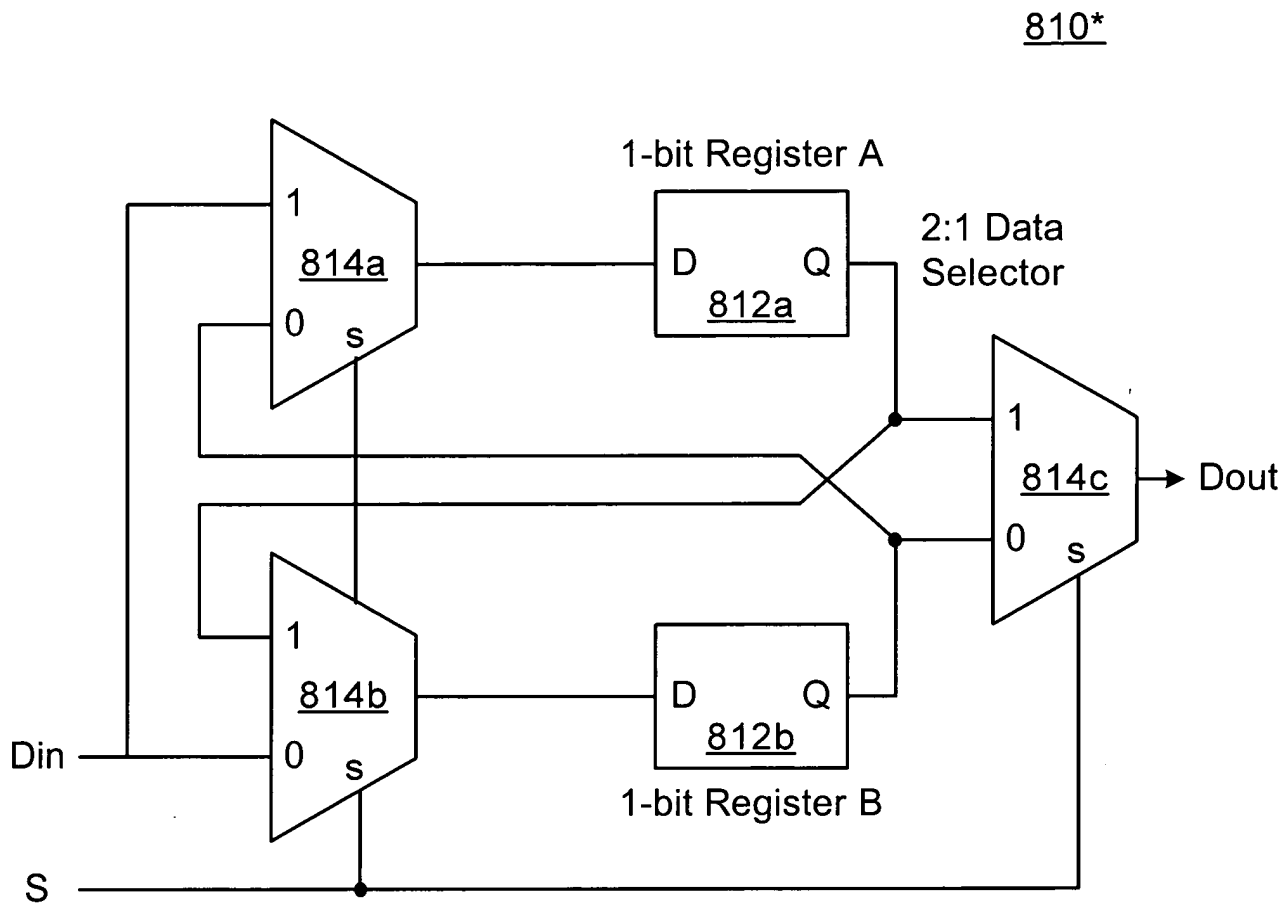
810*
1-bit Register A
1
814a
0
s
D
Q
812a
2:1 Data
Selector
1
814c
0
s
Dout
1
814b
0
s
Din
D
Q
812b
1-bit Register B
S

FIG. 4c